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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,984	08/11/2000	Bruce Harmon	SYNOPSYS-00701	8482

35273 7590 03/03/2004

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EXAMINER	
BARNES, CRYSTAL J	

ART UNIT	PAPER NUMBER
2121	17

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/637,984	HARMON ET AL.	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-14,17-24,27 and 28* is/are rejected.

7)☒ Claim(s) *6,7,15,16,22,23,25,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3,13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending in the application.

Priority

2. Applicant has complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119(e). Applicant's claim for domestic priority under 35 U.S.C. 119(e) is granted.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 04 December 2000 and 19 April 2002 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

4. The drawings are objected to because reference number 879 in figure 2 should be reference number 819 (see page 9 lines 12, 14). A proposed drawing correction or corrected drawings are required in reply to the Office action to

avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities: peripheral device 208 on page 12 line 17 should be peripheral device 834 as shown in figure 1. Appropriate correction is required.

6. The abstract of the disclosure is objected to because a space should be inserted between "simulatorcircuit" on page 22 line 11. Correction is required. See MPEP § 608.01(b).

Claim Objections

7. Applicant is advised that should claims 11 and 17 be found allowable, claims 22 and 23 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in

wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 11, 22 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 11 and 22 recite the limitation "the bus functional model" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

11. Claims 11 and 22 recite the limitation "the hardware model" in lines 4-5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 22 recites the limitation "the processor" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 22 recites the limitation "the internal bus" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 28 recites the limitation "the microcontroller". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 11-14, 17-19, 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,768,567 to Klein et al.

As per claim 11, the Klein et al. reference discloses a hardware model containing the integrated circuit having a processor and internal bus, including: means for disabling the processor (see column 4 lines 39-53, "by-passing hardware simulation 12"); means for allowing a direct communication between the bus functional model (see column 6 lines38-44, "bus interface models 14") and the hardware model ("ISS 20") to send interrupt service routines without passing through the processor (see column 6 lines 9-14, "logic simulators").

As per claim 12, the Klein et al. reference discloses the integrated circuit is a microcontroller (see column 5 lines 29-32, "microprocessors").

As per claim 13, the Klein et al. reference discloses the microcontroller is a Motorola MPC860 (see column 5 lines 29-32, "Motorola Corporation 68030").

As per claim 14, the Klein et al. reference discloses the means for disabling the processor of the hardware model (see column 10 lines 5-10, "by-passing the processor instance") requires the core of the processor to not execute any code (see column 10 lines 11-24, "wait states").

As per claim 17, the Klein et al. reference discloses the internal bus (see figure 2) of the integrated circuit (see column 5 lines 25-27, "hardware-software simulator 10'") may be temporarily uncoupled from the hardware design (see column 6 lines 1-4, "ISS 20, software designs 21, software simulation 18'") so that initialization of the operating system (see column 4 lines 45-48, "optimized accesses are performed directly") only communicates with the instruction set simulator (see column 6 lines 1-14, "ISS 20").

As per claim 18, the Klein et al. reference discloses a system for modeling a hardware design for carrying out an operation wherein the hardware design includes an integrated circuit having a processor and an internal bus; the system

comprising: a simulator circuit (see column 5 lines 25-27, "hardware-software simulator 10'") simulating the hardware design (see column 5 lines 57-59, "hardware design 32") and including the integrated circuit ("hardware-software simulator 10'"); an instruction set simulator (see column 6 lines 1-4, "ISS 20") for representing an operation of the processor (see column 6 lines 9-10, "logic simulators"); and means for disabling the processor (see column 4 lines 39-53, "by-passing hardware simulation 12").

As per claim 19, the Klein et al. reference discloses the simulator circuit comprises: a hardware model (see column 5 lines 57-59, "hardware simulation 12'") containing the integrated circuit (see column 5 lines 25-27, "hardware-software simulator 10'") having the processor ("logic simulator 13") and the internal bus (see figure 2); a bus functional model (see column 5 lines 25-38, "bus interface models 14") for interfacing the instruction set simulator (see column 6 lines 38-44, "ISS 20") to the simulator circuit ("hardware-software simulator 10'") wherein the simulator circuit ("hardware-software simulator 10'") can carry out the operation without intervention of the processor ("logic simulator 13") for determining whether the hardware design (see column 5 lines 57-59, "hardware design 32") is correct; and a transfer memory (see column 5 lines 39-56, "memory models 16") to

pass system interrupts between the hardware model (see column 5 lines 57-59, "hardware and software simulations 12, 18") and the bus functional model (see column 5 lines 29-38, "bus interface models 14").

As per claim 22, the rejection of claim 11 is incorporated and further claim 22 contains limitations recited in claim 11; therefore claim 22 is rejected under the same rationale as claim 11.

As per claim 23, the rejection of claim 17 is incorporated and further claim 23 contains limitations recited in claim 17; therefore claim 23 is rejected under the same rationale as claim 17.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,768,567 to Klein et al. in view of logical reasoning.

As per claim 1, the Klein et al. reference discloses a system for modeling a hardware design for carrying out an operation wherein the hardware design includes: an integrated circuit (see column 5 lines 25-27, "hardware-software simulator 10'") having a processor ("logic simulator 13") and an internal bus (see figure 2); a hardware model (see column 5 lines 57-59, "hardware simulation 12'") containing the integrated circuit ("hardware-software simulator 10'"); a bus functional model (see column 5 lines 25-38, "bus interface models 14") employing a first system interface unit and a second system interface unit (see column 6 lines 38-44, "one of the bus interface models 14, an ISS 20"); means for disabling the processor of the integrated circuit (see column 4 lines 39-53, "by-passing hardware simulation 12"); means for simulating the operation of the processor (see column 4 lines 33-37, "hardware and software simulations 12, 18"); and means for modeling the internal bus of the integrated circuit ("bus interface models 14") and providing signals which would ordinarily appear on the internal bus of the hardware design (see column 6 lines 1-4, "ISS 20").

The Klein et al. reference does not expressly disclose a bus functional model employing a first system interface unit and a second system interface unit.

However, it would have been logically to one of ordinary skill in the art to modify the manner in which the bus interface models 14 cooperated with other elements.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to associate the plurality of processor bus interface models with the first and second system interface units.

One of ordinary skill in the art would have been motivated to modify the bus interface models so that each bus interface models associated/communicated with a particular element of the hardware-software co-simulator.

As per claim 2, the Klein et al. reference discloses the integrated circuit is a microcontroller (see column 5 lines 29-32, "microprocessors").

As per claim 3, the Klein et al. reference discloses the microcontroller is a Motorola MPC860 (see column 5 lines 29-32, "Motorola Corporation 68030").

As per claim 4, the Klein et al. reference discloses the first system interface unit of the bus functional model (see column 6 lines 38-44, "one of the bus interface models 14, an ISS 20") communicates over an external bus to the hardware design (see column 6 lines 1-4, "ISS 20, software designs 21, software simulation 18'"), and the second system interface unit of the bus functional model

("one of the bus interface models 14, an ISS 20") communicates with the hardware model (see column 5 lines 57-59, "hardware simulation 12'").

As per claim 5, the Klein et al. reference discloses the means for disabling the processor of the hardware model (see column 10 lines 5-10, "by-passing the processor instance") requires the core of the processor to not issue any bus cycles (see column 10 lines 11-24, "wait states").

As per claim 8, the Klein et al. reference discloses the means for simulating the operation of the processor (see column 6 lines 16-17, "hardware-software co-simulation 10'") is accomplished such that the functional behavior of the system is provided through a combination of hardware and software (see column 22-24, "hardware and software simulations 12, 18").

As per claim 9, the Klein et al. reference discloses at least some of the software-provided functional behavior is provided by an instruction set simulator (see column 6 lines 1-4, "ISS 20").

As per claim 10, the Klein et al. reference discloses at least some of the software-provided functional behavior is provided by the bus functional model (see column 6 lines 38-44, "bus interface models 14").

19. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,768,567 to Klein et al. as applied to claims 18 and 19 above, and further in view of logical reasoning.

As per claim 20, the Klein et al. reference does not expressly disclose the hardware model simulates the integrated circuit by communicating with the bus functional model through a system interface unit.

However, it would have been logically to one of ordinary skill in the art to modify the manner in which the bus interface models 14 cooperated with other elements.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to associate the plurality of processor bus interface models with the first and second system interface units.

One of ordinary skill in the art would have been motivated to modify the bus interface models so that each bus interface models associated/communicated with a particular element of the hardware-software co-simulator.

As per claim 21, the Klein et al. reference discloses the instruction set simulator (see column 6 lines 1-14, "ISS 20") is external to the simulator circuit

(see column 5 lines 57-59, "hardware simulation 12'") and executes interrupt service routines (see column 11 lines 50-56, "stop simulation interrupt").

20. Claims 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,911,059 to Profit, Jr. in view of USPN 5,768,567 to Klein et al.

As per claim 24, the Profit, Jr. reference discloses a method of modeling an integrated circuit, comprising the following steps: putting a central processing unit (CPU) into an inactive state; servicing an instruction set simulator (ISS) access into peripheral devices; servicing peripheral-generated cycles (see column 12 lines 39-42, "periodic request for service"); and servicing peripheral-generated interrupt requests (see column 12 lines 36-39, "services interrupts").

The Profit Jr. reference does not expressly disclose putting a central processing unit (CPU) into an inactive state and servicing an instruction set simulator (ISS) access into peripheral devices.

The Klein et al. reference discloses

(see column 4 lines 45-48, "... optimized accesses are performed "directly", by-passing hardware simulation 12.")

(see column 6 lines 4-6, "ISS 20 ... memory access libraries ... for calling co-simulation optimization manager 27 to perform memory accesses.")

(see column 6 line 42, "... establishing optimized memory access address ranges ...")

(see column 6 lines 56-61, "... compiled executable code linked with memory access library routines ... ISS 20 for calling co-simulation optimization manager 27.")

(see column 12 lines 19-26, "... co-simulation optimization manager 27 retrieves the requested data directly, by-passing hardware simulation ... no-ops for the hardware simulation ...")

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method and apparatus for testing software taught by the Profit, Jr. reference with the optimizing hardware and software co-simulator taught by the Klein et al. reference to provide both hardware and software simulations for electronic systems.

One of ordinary skill in the art would have been motivated to incorporate an instruction set simulator and a co-simulation optimization manager into one system

to provide high-speed processing for both hardware and software simulations of electronic systems.

As per claim 27, the Profit, Jr. reference discloses the integrated circuit is a microcontroller (see column 6 lines 5-11, "microprocessor-based device").

As per claim 28, the Klein et al. reference discloses the microcontroller is a Motorola MPC 860 (see column 5 lines 29-32, "Motorola Corporation 68030").

Allowable Subject Matter

21. Claims 6, 7, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to in general:

USPN 6,298,320 B1 to Buckmaster et al.

USPN 6,279,146 B1 to Evans et al.

USPN 6,212,489 B1 to Klein et al.

USPN 6,052,524 to Pauna

USPN 5,838,948 to Bunza

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 703.306.5448. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anil Khatri can be reached on 703.305.0282. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cjb
February 23, 2004

ANIL KHATRI
SUPERVISORY PATENT EXAMINER